REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed October 8, 2009. Applicants have amended claim 1 and hereby submit the presently pending claims 1-4, 13 and15 are in their allowable forms.

Discussion of the claim rejection under 35 USC 102

Claims 1, 3, 4 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (5,982,601).

In claim 1 of the application, the first connection terminal (of the SCR) is connected to the I/O pad, and the fourth connection terminal (of the anti-latch-up circuit) is directly connected to a voltage source.

Lin discloses VH (alleged common horizontal line) can be PAD or VDD bus (Fig. 6C). Regarding PAD, Lin doe not particularly point out what kind of the PAD it is, but Lin fails to point out that the PAD in Fig. 6C is an I/O pad. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. But, Lin fails to teach the first connection terminal (of the SCR) is connected to the "I/O pad", and thus the 102 rejection is improper.

In addition, the examiner alleged that "the first connection terminal line and the fourth connection terminal line of Lin are connected to one common horizontal line which branches out to the I/O pad and the voltage source according to the office action (*on page 10, second paragraph, in the Office Action*)".

Based on the very basic circuitry theory, the terminals connected to the same line (sharing the same node VH) have the same voltage level. Therefore, based on the examiner's understanding of the Lin reference, the first connection terminal line and the fourth connection terminal line (both of the Lin reference) should be provided with the same voltage.

If following the assumption of the examiner's understandings, the alleged PAD (branched out from the horizontal line) is the I/O pad, and the PAD 100 is further connected to a voltage source, then the voltage source (high level) is constantly provided to the SCR 112 (use the alleged element to apply to claim 1 of the application) and as a result the SCR 112 is always turned on. Under the examiner's interpretation, during the normal operation, the Lin's SCR 112 is still activated. As a result, Lin failed to disclose "wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation" of claim 1.

According to MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987).

Thus, claim 1 is not anticipated by Lin, and the rejection under 35 U.S.C. 102(b) should be withdrawn.

Claim 3 depends on claim 1, and should be patently distinguishable over Lin for at least the reasons above that claim 1 is not anticipated by Lin.

Claim 4 further discloses the anti-latch-up circuit comprises a capacitor and a resistor,

where the capacitor has a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage; and the *resistor has a first end and a second end, respectively coupled to the voltage source and the second N+ doped region*.

According to Lin, the RC circuit is a part of the transient oscillator 61, and comprises a capacitor C2 and a resistor R2 (referring to Fig. 6C). The capacitor C2 is connected between VH (not ground) and a node (connected to a gate of a transistor M2, but not a N+ doped region of the SCR circuit). The resistor R2 is connected between the node and VL (not a voltage source). Therefore, the RC circuit disclosed in claim 4 is different from the connection of Lin's RC circuit, and not anticipated by Lin.

According to MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Thus, Lin failed to disclose the connection as disclosed by claim 4 of the application, and the rejection under 102(b) is improper. Therefore, claim 4 is patently distinguishable over and not anticipated by Lin.

Claim 13 depends on claim 1, and should be patently distinguishable over Lin for at least the reasons above that claim 1 is not anticipated by Lin.

In summary, since claims 1, 3, 4 and 13 are not anticipated by the Lin reference, the rejection under 35U.S.C. 102 (b) should be withdrawn and claims 1, 3, 4 and 13 should be allowed.

Discussion of the claim rejection under 35 USC 103

1. Claims 1, 3-4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley (5,781,388) in view of Lin (5,982,601). In addition, claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

On page 5 in the Office Action, the examiner stated "*Quigley does not explicitly state that the voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latch-up of the SCR circuit during the normal operation…*", but Lin teaches in figures 6, 9 and 10 and related text such features.

However, for the reasons discussed in above for the 102 rejection, if following the assumption of the examiner's understandings, the alleged PAD (branched out from the horizontal line) is the I/O pad, and the PAD 100 is further connected to a voltage source, then the voltage source (high level) is constantly provided to the SCR 112 (use the alleged element to apply to the present invention) and as a result the SCR 112 is always turned on. Under the examiner's interpretation, during the normal operation, the Lin's SCR 112 is still activated. As a result, Lin failed to disclose "wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation" of claim 1.

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." In re Lalu, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

However, since Lin fails to disclose "*the voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latch-up of the SCR circuit during the normal operation...*", even though Quigley combines Lin's teachings, the alleged combination still fails to disclose claim 1 feature of the application. Therefore, the rejection under 103(a) for claim 1 of the application is improper.

In summary, neither the Quigley nor Lin reference discloses the claimed features recited in claim 1 of the invention. Even though Quigley uses the teachings of Lin, the alleged combination still fails to disclose the claimed features of the invention. There, claim 1 is not obvious over Quigley in view of Lin, and the rejection under 35 U.S.C. 103(a) should be withdrawn.

Also, the remaining claims 3, 4, 13 and 15 depend directly or indirectly from the proposed independent claim 1, and therefore patently define over Quigley and Lin for at least the reasons cited above.

Regarding claim 4, the examiner's alleged that Lin teaches in figure 6C an anti-latch-up circuit comprises a capacitor and a resistor. However, for at least the same reasons discussed in above 102 rejection for claim 4, Lin failed to disclose a capacitor has a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage and a resistor has a first end and a second end, respectively coupled to the voltage source and the second N+ doped region as disclosed in claim 1 of the application. Therefore, claim 4 is patently distinguishable over Lin.

For at least the same reasons discussed above, claim 15 is patently distinguishable over Lin, and the rejection should be withdrawn.

2. Claim 2 is rejected under 35 U.S.C 103(a) as being unpatentable over Quigley and Lin and further in view of Ker et al. In addition, claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Ker et al (5,754,380).

The disclosures of Quigley and Lin are discussed above. Ker discloses a COMS output buffer with enhanced high ESD protection capability, in which diodes 60 and 70 are serially connected between power lines VDD and VSS to serve as discharge pathways.

However, as discussed above, since Lin, Quigley or Quigley in view of Lin fails to disclose the claimed circuit structure, even though Lin or Quigley uses the Ker's teachings to insert the diode string between power lines VDD and VSS, the alleged combination still fails to disclose claimed structure as disclosed in claim 2 of the application.

As a result, claim 2 is patently distinguishable over Lin in view of Ker, or over Quigley in view of Ker, and the rejection should be withdrawn.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4, 13 and 15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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/JIAWEI HUANG/
Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809
Email: jcpi@msn.com